CLAIM

1) "WIRELESS TELEPHONE EQUIPMENT WITH SPECTRAL SPREAD IN SAMPLED VOICE", characterized for being composed of base and portable (handset), being that both use transmitters and receivers with the "Spectral Spread in Sampled Voice" concept whose diagrams in sections and wave forms are shown in figures (3A), (3B), (4A) and (4B), and that present diagrams of the portable set and base as shown in Figures (1) and (2) respectively, and because they use transmitter and receiver under the "Spectral Spread in Sampled voice" concept, allow reduction in battery consumption and discard the need to operate in distinct bands for transmission and reception in relation to wireless telephone using spectral spread in analog voice, and that for not digitizing voice presents the advantage of not needing analog/digital converters, level quantifier circuits, generating considerable reduction in costs and for allowing small time delays in transmission and reception discards use of echo canceling circuits, as used by digital phones which spread or not the frequency spectrum, allowing for raw material costs reduction.

2 - "WIRELESS TELEPHONE EQUIPMENT WITH SPECTRAL SPREAD IN SAMPLED VOICE" according to claim in 1, characterized by a transmitter which allows its application in any transmission equipment of analog signals by radio, and that consists of sampling the signal to be transmitted through Sample-and-Hold (S/H), limiting the duration of each sample to the transmission pulse duration and making them modulate in one carrier frequency during the transmission pulse, which is simultaneously modulated in phase by PN sequence that promotes spectral spread of transmitted signal in direct sequence, which presents delay in hundreds of micro-secs, quite shorter than that caused by transmitters that digitize voice, and therefore allowing the manufacturing of wireless phones and PABX without echo canceling circuits and for their transmitting in short interval allow turning reception off for the user to receive signals in the same frequency, eliminating the need for duplexers and two distinct bands for transmission/reception in a given equipment, and which shall operate

in sync with the receiver under the concept of "Spectral Spread in Sampled Voice", and that in conjunction with the "Spectral Spread in Sampled Voice" enables greater communication range under the laws in force regulating and allowing greater power for equipment using spectral spread transmission.

3 - "WIRELESS TELEPHONE EQUIPMENT WITH SPECTRAL SPREAD IN SAMPLED VOICE" with receiver having an internal PN generator that generates three sequences, PNE, PNL and PNi. This last one in sync with PN within the signal received called PNrx. This synchronism is done by the circuit called DLL (delay locked loop); PNE (E for Early) and PNL (L for late) are exact replicas of PNi, but PNE is advanced by half a chip in relation to PNi, and PNL late by half a chip in relation to PNi.; DLL functioning is based on behavior of the PNs autocorrelation function. PN is a maximum sequence code whose autocorrelation presents the behaviors shown in figure (5). The PN autocorrelation, when $|\tau|>1$chip (phase difference greater than a chip), is always constant with value equal to minus one. When $\tau = 0$ (phase signal), autocorrelation value is maximum and equal to the total number of PN chips . When $-1<\tau<1$, i.e. when the difference of phase b/w signals is within the range of plus one or less one chip, the autocorrelation value varies linearly due to τ; it is also observed in the figure that the autocorrelation value is the same for $\tau = ½$ chip and for $\tau = - ½$ chip. For that reason the PNi generator also generates PNE and PNL signals. When PNrx is in phase with PNi, PNrx is delayed by half chip ($\tau = -1/2$ chip) in relation to PNE and advanced by half chip ($\tau = ½$ chip) in relation to PNL. This is the only condition (considering the range $-1<\tau<1$) in which the output levels of the two band pass filters of the DLL present the same output level. It is also the DLL stabilization condition, i.e. the DDL condition it should be in when the receiver is ready for reception. This condition is commonly known as lock in PLL circuit analogy (phase locked loop); When PNrx is not in phase with PNi but the phase difference phase is within more or less one chip, this means that PNrx is either less dephased from PNE or more dephased from PNL, or otherwise. That, therefore, means that the output band pass filter levels of the

DLL will be different and at the output of the adder there will be a signal of error that will increase or decrease the frequency of the VCO clock, advancing or delaying PNi, PNE and PNL in relation to PNrx to force correlation b/w PNrx and PNL to be equal to correlation b/w PNrx and PNE (PNE advanced by ½ chip and PNL delayed by ½ chip, both in relation to PNrx) and when that happens, the lock state is reached; when the phase difference between PNrx and PNi is greater than one chip, the band pass filters output level of the DLL shall have the same value, generating an error signal equal to zero; The DLL will acts as if in lock and will not try to put PNrx in phase with PNi; In that case, what took place is a false DLL lock. To know if the lock is real or false, verify correlation b/w PNrx and PNi. When the lock is real, correlation is maximum and band pass filter output level of the despreader is maximum; When the lock is false, it is minimum and the filter output is minimum; As soon as the receiver is connected, despreader output shows a tension level that varies according to the degree of correlation b/w PNrx and PNi; As the communication channel, at first, introduces an unknown delay at PNrx, it is not possible at first to determine the difference in phase b/w PNrx and PNi; when the dephasing b/w two signals exceeds the range by more or less one chip, correlation b/w the two signals is minimum and the despreader output is minimum; When dephasing is zero, correlation b/w these signals is maximum and the output level is maximum; If the difference in phase b/w signals is of more or less ½ chip, the correlation value b/w the signals is of 50% the difference b/w minimum and maximum correlation; That means that the despreader output level will also be half the difference b/w the greater and the lower output level; This level is called voltage threshold (Vt) and applies to a voltage exactly equal to this one at the reference input of the voltage comparator; The other input of the comparator will receive output signal from the despreader; Thus, when dephasing b/w PNrx and PNi exceeds the range of more or less ½ chip, the comparator input levels is less than Vt and the output voltage of the comparator stays at low level; When dephasing b/w PNrx and PNi is within the range of more or less ½ chip, the comparator input level is greater or equal to Vt

and the output level of the comparator goes to high level (one); there is delay of one chip in PNi, PNL and PNE every sampling period while the output voltage comparator is "zero" ;we must force the system for the dephasing b/w PNrx and PNi to stay within the range of more or less ½ chip for the DLL to reach lock state; Thus, when dephasing b/w PNrx and PNi is of various chips and one and one chip every sampling period until reaching dephasing within range of more or less ½ chip; When that occurs, the output level of the tension comparator goes to high level and the PN generator stops creating one chip delays; At that moment, DLL starts to act in VCO frequency until lock state is reached, i.e.; until the phase difference b/w PNrx and PNi is kept next to zero; three distinct states of the receptor can be defined: acquisition, tracking and lock; In sequence of receptor functioning, the 1st state is acquisition, the state of reception start, when dephasing b/w PNrx and PNi exceeds range or more or less ½ chip, the PN generator creating one chip delays every sampling period and output voltage of comparator zero; Tracking occurs next when dephasing b/w PNrx and within more or less ½ chip, comparator output goes to high and PN generator stops one chip delay. Lock comes next and then PNi accompanies within given limitations, PNrx phase variations to keep dephasing b/w these signals close to zero; allowing the functioning of receptions of the "Wireless Telephone Equipment with Spectral Spread in Sampled Voice" according to claim 1, which is characterized by receptor with new concept called "Spectral Spread in Sampled Voice" shown o figures (4A) and (4B), which allows for its use in any equipment of analog signal reception via radio and that consists of receiving a signal from transmitter from Claim 2 , eliminate spectral spread through correlation of signal received with PN sequence generated internally, which is synchronized with the signal received through DLL circuit (Delay Locked Loop) or any other synchronism circuit based on autocorrelation of PN sequences and that at despreader circuit output presents a carrier modulated in frequency by the information samples transmitted and modulated in amplitude by the transmission pulse, and which demodulates this carrier in FM, obtaining ate demodulator

output pulses whose amplitude vary due to transmitted information level, and which through such pulses, using a sampling circuit and a band pass filter, restores transmitted analog signal through transmitter, and from zero dephasing information b/w PN sequence of signal received and PN sequence generated locally, the detector circuit involving the despreader output and the synchronizer, obtaining clock signal necessary to sample, and which allows a sensitivity of about 7 dB worse than a conventional FM receiver as shown in the simulation presented in this patent request limited to example purposes only, which should operate in sync with the transmitter of claim 2, and operating in unison with the transmitter set of claim 2 allows for greater communication range.